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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PRIETO, BEATRIZ	

ART UNIT	PAPER NUMBER
2142	

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,116	DERR, MICHAEL N.	
	Examiner	Art Unit	
	Prieto B.	2142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/19/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3 and 5-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3 and 5-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Amendment filed 12/19/05, claims 2-3, 5-25 remain pending and have been examined.

2. Amendment to claims 14-15, 18 and 19 with respect to the use of an acronym IDE, is acknowledge, previous objection is hereby withdrawn.

Claim Rejection under 103

3. Quotation of the appropriate paragraphs of 35 U.S.C. 103 that form the basis for the rejections under this section made in this Office action may be found in previous office action.

4. Claims 2-3, 5-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over BAKER (US 5,996,032) in view of RUNALDUE et. al. (US 5,999,441) (referred to as Runaldue hereafter).

Regarding claim 12, Baker teaches a computer (Fig. 1) comprising:

a processor subsystem supported by bus 24 & 26 (Fig. 1);

a device (18), which transfers data to or from, said processor subsystem (col 10/lines 54-57, and col 5/lines 35-39) and a device (14), which transfer data to/from said processor (col 7/lines 38-48, col 6/lines 3-14 and col 21/lines 50-56);

a controller (20) adapted to control the transfer of data between said device and said subsystem (col 5/lines 20-45); and

writing in a register only the bits at the bit locations in the register for with the enable bit in the corresponding location in the bit enable field is set with the corresponding location in the data field (abstract, col 10/lines 60-col 11/line 20, col 16/lines 44-52);

receiving a data value of a write command to a register in the controller (abstract);

processing "interpreting" bits of the data value as enable bits in a bit enable field which designate predetermine bits within the register to which data is to be written and writing data only to the predetermined bits in a register write operation using a single write enable command (column 3, lines 15-27);

however does not explicitly teach where the number of enable bits in the bit enable field is the same as the number of bits in the register where the data is to be written.

Runaldue teaches writing individual bits of data to a "register" memory (10) (col 1/lines 14-17, 60-64 and col 2/lines 51-56), said method comprising:

receiving bits of input data in a data field (DATA [0:7]) to be stored in said register, the register composed of memory cells (12) arranged in eight columns [0:7] (14), thereby the number of bits in said input data field being equal to the number of bits in the register and bit locations in the data field corresponding respectively to "bit locations" addresses in the register (Fig. 1, and col 3/lines 30-57);

receiving enable bits in a bit enable field (BIT_EN) from logic (18), the number of enable bits in the bit enable field being equal to the number of bits in the register and "bit locations" addresses in the bit enable field corresponding respectively to "bit locations" addresses in the register (col 3/lines 65-col 4/line 5, col 5/lines 28-29 and col 1/lines 19-41), and

overwriting only the bits at the bit locations of the register according to the write enable bits in the write enable field (WRTDAT) for which the enable bit in the corresponding location in the bit enable field is set with the bit of input data in the corresponding location in the data field (col 2/lines 7-12, 20-32).

It would have been obvious to one ordinary skilled in the art at the time the invention was made given the suggestion of Runaldue for applying the his teachings to application using random access memory for storing data having multiple configuration lengths, the applicability to Baker environment including PC cards, i.e. memory cards, e.g., a SRAM (Static Random Access Memory) card, ROM (Read Only Memory) card, using IEEE 1394 standard communication (and suggesting the use of other different types of communication buses), typically used for communicating via telephone lines, a LAN card for connecting PCs via LAN, a SCSI (Small Computer System Interface) card for connecting to a SCSI apparatus, a sound card for playing music or producing sound effects by a PC, an ISDN (Integrated Services Digital Network) card for connecting to ISDN lines, and a Video Capture card for capturing a video signal. Motivation to combine would be modify data, such as individual bits of an addressed word within a single clock, reducing latency.

Regarding claim 13, an interconnecting device/means "bridge" (20 or 34) between the processor subsystem and at least said device, the controller being included in the switch or multiplexing function device (Baker: col 30/lines 22-54 Fig. 26a).

Regarding claim 14, wherein the device comprises an storage device (Baker: 22) and the bridge comprises an "I/O controller hub" (ICH), which controls an IDE data, transfer between the processor subsystem and the IDE storage device (Baker: col 30/lines 22-54 Fig. 26a).

Regarding claim 15, this claim is substantially the same as claim 10, same rationale of rejection is applicable.

Regarding claim 16, this claim comprises the software program stored in a tangible medium, said program, when executed, causing a computer to execute a method of claim 1, discussed above, same rationale of rejection is applicable.

Regarding claim 17, wherein said software program comprises a driver in the operating system software executed by a processor subsystem in the computer (Baker: host processor 44).

Regarding claims 18-19, this claim is substantially the same as combined limitations claims 1-3, and 9-10, same rationale of rejection is applicable

Regarding claims 2-3, wherein the register is a "control" register for a data transfer operation (BAKER: 58 on Fig. 2 control and status registers), including transfers data to or from an storage device (Baker: data transfer to or from said processor subsystem col 10/lines 54-57, and col 5/lines 35-39) and data transfer to/from said processor col 7/lines 38-48, col 6/lines 3-14 and col 21/lines 50-56);

Regarding claim 5, wherein the control register is an "IDE DMA" status register (Baker: 76 on Fig. 2), and wherein the control register is a command register (Baker: col 17/line 66-col 18/line 50).

Regarding claims 6-8, wherein some of the bits of said register are not overwritten (Runaldue: col 2/lines 25-32), wherein the data field and the bit enable field are received in parallel (Runaldue; col 2/lines 14-25) and wherein the data field is provided at an address which is contiguous with the address for the bit enable field (Runaldue: 7-bit address signal (ADDR) [0:7] of Fig. 1, i.e. continuous).

Regarding claim 9, wherein the data transfer operation comprises an IDE data transfer between a processor subsystem and an external IDE storage device (137) (Runaldue: Fig. 2).

Regarding claim 10, wherein the processor subsystem posts an entire command sequence for setting up the IDE data transfer (Baker: col 14/lines 64-66).

Regarding claim 11, wherein the method is carried out in controller in a interconnecting device or means connected between the processor subsystem and the external IDE storage device or peripheral supporting all data transfers therein (Baker: col 6/lines 39-59).

Regarding claim 20, the combined teachings as discussed above, further teach

receiving data of a single write command wherein the received data comprises a "data" input write data field (252) comprising an arbitrary number of bits, a write strobe signal (264), and an address bit field [1:4] (266) of a register where data is to be written, and an write enable bit (258) comprising a predetermine number of bits,

the outputted write command data (270) comprising: the address bit field (272) comprising a register address bit (274) and an individual bit select field (276) addresses bits (Fig. 10);

modifying or changing the register with one or more bits of the data field that are associated with the enable bits of the bits enabled field (Baker: col 16/line 32-col 17/line 10).

Regarding claim 21, where the data (270) of the single write command comprises at least two bits (Baker: 1 to 4 GPIOs to be written, col 16/lines 53-55), the write enable field (258) comprises one or more bit, and the input write data field comprises any number of bits (Baker: col 16/lines 32-46).

Regarding claims 22-25, register has location in a logical space and a physical space (Runaldue: column 1, lines 19-41), single write command (Baker: abstract); write of data value to a space in the register (Baker: abstract); the data value comprises a number of enable bits that correspond to the same number of bits of the register (Runaldue: column 1, lines 14-41; column 2, lines 3-6, 49-56, and column 3, lines 50-57).

Response to Arguments

5. Regarding at least claim 12, it is argued (p. 9-10) that Baker nor Runaldue teach receiving data of a single write command wherein the data comprises a bit enable field and a data field having same number of bits in each bit enable field and data field.

In response to the above-mentioned argument, applicant's interpretation of the applied art has been considered. Corresponding claim limitation as amended reads, receiving a data value of a write directed to a control register in the controller, interpreting bits of the data value as a data field, the number of bits in the data field being equal to the number of bits in the control register in the controller and bit location in the data field corresponding respectively to bit locations in the control register. Baker discloses:

> Register write circuitry (250) writes to a plurality of data register bits (276) using a single register write operation by storing both designated address bits (276) and an address field (274) for addressing a predetermined data register. The designation address bits (276) designate predetermined bits (A_4,A_2,A_2,A_1) within data register (76) to which data was to be written. Writing data (274) only to predetermined bits (276) in a register write operation uses a single write enable command (272) in a programmable and selectable manner without performing a read-modify-write or requiring the storage of a bit image of the register (see abstract). FIFO Control and Status Registers 88 implement the control and status register set of the FIFO logic 78. This register is accessed via a PCI-slave 66 read or write operation (column 9, line 41-48). Provided a method and system for writing a plurality of data register bits that uses a single register write operation, including storing both designation address bits in an address field for addressing a predetermined data register, which designates predetermined bits within the data register to which data is to be written as active and other bits within the data register as inactive. Writing data only to the predetermined bits in a register write operation using a single write enable command (column 3, lines 15-27).

Baker teaches receiving a data value of a write command directed to a control register in the controller, interpreting bits of the data value as a data field, and a bit enable data field, writing in the register only the bits at the bit location in the register for which the enable bit in the corresponding location is set with the corresponding location in the data field. Runaldue teaches

> The present invention relates to apparatus and methods for writing a selected bit of a word into a random access memory (RAM) having a prescribed number of bits defining a word length (column 1, lines 14-17); Hence, the reading and writing of data to and from a memory array involves addressing a word of memory based on its corresponding address, and reading and/or writing the word having the prescribed number of bits from the memory array (column 1, lines 37-41); enabling selected bits of a data word to be selectively written into a random access memory without overwriting other non-selected bits of the data word stored in the memory (column 2, lines 3-6); control logic enables selected bits of an addressed word to be written to, without overwriting unselected bits in the addressed word. Hence, individual bits of an addressed word may be modified within a single clock cycle, without the necessity of performing a read-modify-write sequence of operations requiring at least three clock cycles plus external logic to manipulate the individual bits of the addressed word (column 2, lines 49-56); According to prior art techniques, applications requiring setting or resetting of a specific bit within an addressed word would require the entire data word (e.g., bits C0-C7 of a selected row) to be output using a sensing circuit (not shown), modifying the selected bit using external logic, and rewriting the word having the modified bit back into the addressed memory location on a word-by-word basis (column 3, lines 50-57). The address decoder 16 is configured as a conventional 128 by 8-bit decoder, where the address decoder 16 asserts a selected one of the word lines (WORDLN[0:127]) in response to the 7-bit address signal (ADDR). The address decoder also asserts the bit line B, B# (i.e., "NOT B"=B#) on each of the columns 14. Hence, the RAM 10 may operate as a conventional memory, where each bit of the input data (DATA[0:7]) is written into a corresponding column array 14 at a selected row specified by a corresponding one of the word lines (WORDLN) and in response to the write enable signal (WE) (column 3, lines 30-57).

Runaldue discloses where the enable bit field is of the same number of bits and/or length of the register where data is to be written according to the bits in the enable bit field.

6. Regarding at least claim 20, it is argued (p. 9 of remarks) that Baker does not teach receiving data of a write command wherein that data comprises a bit enable field and a data field comprising same number of bits and then updating a register with one or more bits of the data field that are associated with the enable bits of the bit enable bits.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., sequential steps or acts, where a single write command is received and "then" a register is updated) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In this case, the applied reference seems to discloses a prior art technique, where applications requiring setting or resetting of a specific bit within an addressed word would require the entire data word (e.g., bits C0-C7 of a selected row) to be output using a sensing circuit (not shown), modifying the selected bit using external logic, and rewriting the word having the modified bit back into the addressed memory location on a word-by-word basis (column 3, lines 50-57). The present invention relates to apparatus and methods for writing a selected bit of a word into a random access memory (RAM) having a prescribed number of bits defining a word length (column 1, lines 14-17), as discussed above.

7. Applicant's argument has been fully reviewed but not found persuasive.

8. Reply to a final rejection or action must include cancellation of, or appeal from the rejection of, each rejected claim. If any claim stands allowed, the reply to a final rejection or action must comply with any requirements or objections as to form (see 1.113). If prosecution in an application is closed, an applicant may request continued examination of the application by filing a submission and the fee set forth in § 1.17(e) prior to the earliest of: (c) A submission as used in this section includes, but is not limited to, an information disclosure statement, an amendment to the written description, claims, or drawings, new arguments, or new evidence in support of patentability. If reply to an Office action under

35 USC 132 is outstanding, the submission must meet the reply requirements of § 1.111 (see MPEP 706.07).

9. An amendment filed after final rejection is not entered as a matter of right and must be filed in compliance with 37 CFR 1.116 or 1.312, respectively (see MPEP 201). An amendment that will place the application either in condition for allowance or in better form for appeal may be admitted. Amendments complying with objections or requirements as to form are to be permitted after final action in accordance with 37 CFR 1.116(a) (see MPEP 706.07(e)) may also be admitted. Except where an amendment merely cancels claims, adopts examiner suggestions, removes issues for appeal, or in some other way requires only a cursory review by the examiner, compliance with the requirement of a showing under 37 CFR 1.116(c) is expected in all amendments after final rejection (see MPEP 714.13). .An amendment filed at any time after final rejection, but before an appeal brief is filed, may be entered upon or after filing of an appeal brief provided the total effect of the amendment is to (A) remove issues for appeal, and/or (B) adopt examiner suggestions (MPEP 714.13 see also MPEP § 1207 and § 1211).

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prieto, B. whose telephone number is (571) 272-3902. The Examiner can normally be reached on Monday-Friday from 6:00 to 3:30 p.m. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's Supervisor, Andrew T. Caldwell can be reached at (571) 272-3868. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800/4700.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system, status information for published application may be obtained from either Private or Public PAIR, for unpublished application Private PAIR only (see http://pair-direct.uspto.gov or the Electronic Business Center at 866-217-9197 (toll-free).

Any response to this action should be mailed to:
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March 23, 2006